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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,803	08/25/2003	Eric Chuang	3304.2.80	2347

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MADSON & METCALF
GATEWAY TOWER WEST
SUITE 900
15 WEST SOUTH TEMPLE
SALT LAKE CITY, UT 84101

EXAMINER	
CHAUHAN, ULKA J	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,803	CHUANG, ERIC	
	Examiner	Art Unit	
	Ulka J. Chauhan	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 8-14, 16-18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (APA) [0002] to [0004] and U.S. Patent No. 6,496,193 to Surti et al.

3. As per claims 1-4, 8, and 9, APA discloses:

a core logic unit outputting first image data in a linear mode (Fig. 1 and [0002]: *a core logic unit comprising a north bridge chip 11 and a south bridge chip 12 are used to control data flows among a microprocessor 10, a system memory 13, and a plurality of I/O devices including a graphics card 14... The microprocessor 10 outputs graphing commands to the graphics card 14 via the north bridge chip 11*);

a graphics accelerator in communication with said core logic unit for processing said first image data into second image data in a linear mode (Fig. 1 and [0002]: *The graphics card 14 is electrically connected to the north bridge chip 11 via an AGP bus, and comprises a graphics chip 141*; [0003]: *However, before the graphics chip 141 stores the graphics data into the local memory 142, the graphics data are present in a linear mode*);

a first tile converter in communication with said graphics accelerator for converting said second image data into third image data in a tile mode; a local memory in communication with said first tile converter for storing therein said third image data (Fig. 1 and [0003]: *graphics data*

have to be converted into tile-mode graphics data by the tile converter 143 in advance, and then are stored in the local memory 142);

a system memory accessible by said core logic unit, and comprising a graphics accelerating memory (Fig. 1: *system memory 13 comprising AGP memory block 131*; [0002]: *core logic unit comprising a north bridge chip 11 is used to control data flows among a microprocessor 10, a system memory 13, and a graphics card 14*).

4. APA does not expressly teach: a second tile converter in communication with said core logic unit for converting said first image data into fourth image data in a tile mode, and storing the fourth image data in a tile mode in the graphics accelerating memory within the system memory. This is what Surti teaches. Surti discloses a computer system implementing fast texture loading utilizing a hardware implementation (c. 3 ll. 7-9). Surti discloses a graphics memory controller 12 functioning as a first bridge element between host processor 110, system memory 14, and a graphics memory 13 that is coupled to graphics memory controller 12 via a dedicated graphics bus 24; where the graphics memory 13 and system memory 14 are both arranged as tiled memories (Fig. 1 and c. 3 ll. 10-25). Surti further discloses converting virtual addresses that the host processor is writing to the tiled address space (c. 4 ll. 34-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized Surti's conversion of host processor addresses to tile addresses in combination with APA in order to take advantage of tiled memory architecture which provides efficient method of utilizing memory space and which allows the graphics engine/accelerator to access the AGP memory block in the system memory faster without causing excessive number of page misses, as disclosed by Surti.

5. As per claim 5, APA does not expressly teach that the core logic unit, said graphics accelerator, said first tile converter and said second tile converter are integrated into a single core logic chip. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have integrated the core logic unit, said graphics accelerator, and the first and second tile converters into a single core logic chip in order to achieve faster processing and reduced system cost through integration.

6. Claims 10-14, 16, 17, and 20 are similar in scope to claims 1-5, 8, and 9, and are rejected under the same rationale.

7. As per claim 18, APA does not expressly teach that the first tile converter and said second tile converter are integrated into a single tile converting device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have integrated the first and second tile converters into a single tile converting device in order to reduced system cost through integration.

8. Claims 6, 7, 15, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (APA) [0002] to [0004] and U.S. Patent No. 6,496,193 to Surti et al and U.S. Patent Application Publication No. 2003/0122837 to Saxena et al.

9. As per claim 6, APA does not expressly teach that the local memory is disposed in said system memory. Saxena teaches a computer system utilizing tiled memory architecture in which the system memory is partitioned to create a frame buffer (Fig. 1 and [0032]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented a shared system and graphics memory as taught by Saxena in combination with APA in order to better utilize the available memory space.

10. As per claim 7, APA does not expressly teach that the first tile converter and said second tile converter are integrated into a single tile converting device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have integrated the first and second tile converters into a single tile converting device in order to reduced system cost through integration.

11. Claims 15 and 19 are similar in scope to claim 6, and are rejected under the same rationale.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 20030001853A1 US006856320B1 US006667745B1 US006628294B1

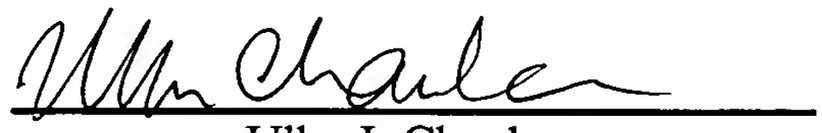
US006072507A US005990912A US005844576A

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ulka J. Chauhan whose telephone number is 571-272-7782. The examiner can normally be reached on Mon. through Fri., 9:30 a.m. to 4:00 p.m.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 571-272-7778. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Ulka J. Chauhan
Primary Examiner
Art Unit 2676

ujc
March 7, 2005